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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/523,900 | 09/22/2005 | Christian Kornblum | 10191/3916 | 7562 |

26646 7590 07/02/2007

KENYON & KENYON LLP
ONE BROADWAY
NEW YORK, NY 10004

| EXAMINER | |
|---|---|
| CHAI, LONGBIT | |
| **ART UNIT** | **PAPER NUMBER** |
| 2131 | |

| MAIL DATE | DELIVERY MODE |
|---|---|
| 07/02/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/523,900 | KORNBLUM, CHRISTIAN | |
| | Examiner | Art Unit | |
| | Longbit Chai | 2131 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *02 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *13-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 February 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/2/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Priority*

1. Applicant's claim for benefit of foreign priority under 35 U.S.C. 119 (a) – (d) is acknowledged.

The application is filed on 9/22/2005 but is a 371 case of PCT/DE03/02309 application filed 7/10/2003 and has a foreign priority application filed on 8/2/2002.

### *Preliminary Amendment*

2. Examiner acknowledges Preliminary Amendment for the claims filed 2/2/2005. Applicants have cancelled claims 1 – 12 and added new claims 13 – 25. The submitted amendments have been entered and made of record. Presently, pending claims are 13 – 25.

### *Claim Objections*

3. Claim 13 is objected to because of the following informalities: "on the basis of the additional information" should be "on a basis of the additional information". Appropriate correction is required.

4. Claim 23 is objected to because of the following informalities: "the at least one data" should be "the at least one data record". Appropriate correction is required.

Any other claims not addressed are objected by virtue of their dependency.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraph of 35 U.S.C. 102 that forms the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 23 and 25 are rejected under 35 U.S.C. 102(e) & 102(b) as being anticipated by Westendorf et al. (U.S. Patent 2002/0042878).

As per claim 23, Westendorf teaches a processor unit (Westendorf : Para [0026] Line 4), comprising:

a buffer memory (Westendorf : Para [0026] Line 7 – 8: a volatile memory is a buffer memory transferred from a data medium drive);

a rewritable functional memory (Westendorf : Para [0028] Line 10 – 13: first data record is transferred from the third processor into the first processor memory) that is accessible during an operation of the processor unit, the buffer memory and the rewritable function memory being capable of storing at least one data record (Westendorf : Para [0026] Line 7 – 8 and Para [0028] Line 10 – 13);

an interface for importing the at least one data record and additional information (Westendorf : Para [0026] Line 11 – 28: i.e. the second data, e.g. a plurality of identity numbers such as processor ID or checksum and etc, can be considered as the

additional information to the first data) into the buffer memory; and a check unit for checking a validity of the at least one data (Westendorf : Para [0035] Line 1 – 6).

As per claim 25, Westendorf teaches the processor unit is a control unit of a motor vehicle (Westendorf : Para [0026] Line 1 and Para [0036] Line 5 – 8).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 13, 14, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grawrock (U.S. Patent 6,678,833), in view of Westendorf et al. (U.S. Patent 2002/0042878).

As per claim 13, Grawrock teaches a method for transcribing at least one data record of an external data source to a processor unit, comprising:

transmitting the at least one data record from the external data source (Grawrock : Column 3 Line 39 – 41, Figure 2 / Element 220 and Figure 3 / Element 340 – 360 & Element 230 : boot block memory unit is external to the TPM (Trusted Platform Module)

processor) together with additional information to a buffer memory of the processor unit (Grawrock : Column 4 Line 3 – 9 and Figure 3 / Element 340 – 360 & Element 230: the modules 340 – 360 can undergo a hash operation to produce corresponding identifiers (e.g., hash identifiers) for later use in verification by a challenger of the processor unit – where the attached hash identifier is interpreted as the additional information).

performing, in the processor unit (Grawrock : Column 4 Line 11 – 13 and Figure 3: the TPM (Figure 3 / Element 230) is considered as the processor unit and the checking is performed by a challenger, which can be located internally to the TPM (i.e. within the processor unit), as taught by Grawrock), a check of an admissibility of a use of the at least one data record on the basis of the additional information (Grawrock : Column 4 Line 8 – 9: hash signatures are used as corresponding identifiers for verification of the received data record).

However, Grawrock does not teach the additional information including an identifier assigned individually to the processor unit; generating a blocking signal when the check indicates that the use of the at least one data record is not allowed; and deleting the at least one data record from the buffer memory; and generating an enable signal when the use of the at least one data record is allowed.

Westendorf teaches:

the additional information including an identifier assigned individually to the processor unit (Westendorf : Para [0026] Line 24 – 26: the identifier could be one of the following – e.g. processor ID or checksum and etc);

generating a blocking signal when the check indicates that the use of the at least one data record is not allowed (Westendorf : Para [0034] Line 30 – 35: output an warning on a display or a loudspeaker and the check process could also be interrupted); and

deleting the at least one data record from the buffer memory (Westendorf : Para [0014] Line 1 – 4); and

generating an enable signal when the use of the at least one data record is allowed (Grawrock: Column 4 Line 36 – 38: the response signal is considered as an enable signal when the use of the at least one data record is allowed).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teaching of Westendorf within the system of Grawrock because (a) Grawrock teaches a data validation method based on a plurality of identities such as hash signatures associated with the desired data records (Grawrock : Column 4 Line 1 – 8) and (b) Westendorf teaches an improved mechanism by including a processor ID as an identifier upon data transfer, besides the checksum, so that it can be determined whether the owner of the processor can be authorized to use the data (Westendorf : Para [0026] Line 24 – 26).

As per claim 14, Grawrock as modified teaches the identifier is valid only once for checking the at least one data record that has been transmitted and stored in the buffer memory (Westendorf : Para [0036] Line 25 – 32: a predetermined period of time of

using the data after validation can be considered as only one time use to meet the claim language).

As per claim 20, Grawrock as modified teaches the processor unit is identifiable by an identity sequence, and the identity sequence is part of the additional information and is used in the check of the at least one data record (Westendorf : Para [0026] Line 11 – 17: i.e. processor ID is also used for validation purpose).

As per claim 21, Grawrock as modified teaches storing valid identifiers for the processor unit in an identifier server (Westendorf : Para [0008] Line 5 – 6 and Para [0030] Line 19 – 24: a database of a central service of office stores identifiers for the processor unit).

7. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grawrock (U.S. Patent 6,678,833), in view of Westendorf et al. (U.S. Patent 2002/0042878), and in view of Alexander et al. (U.S. Patent 6,188,602).

As per claim 15, Grawrock as modified teaches when the enable signal has been generated, the at least one data record is transmitted from the buffer memory to a functional memory from which the at least one data record may be read.

Alexander teaches the enable signal has been generated, the at least one data record is transmitted from the buffer memory to a functional memory from which the at least one data record may be read (Alexander : Column 5 Line 58 – 61: the system

management interrupt signal (SMI) is used to unlock the flash memory for transferring the BIOS information after successful data validation).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teaching of Alexander within the system of Grawrock as modified because (a) Grawrock teaches a data validation method for boot code information update (Grawrock : Column 3 Line 39 – 45) and (b) Alexander teaches an improved and more secured mechanism for boot code update after data validation by locking and unlocking flash memory to enhance the data protection (Alexander : Column 5 Line 58 – 64).

As per claim 16, Grawrock as modified teaches storing the identifier and the at least one data record in the functional memory (Westendorf : Pra [0028] Line 10 – 15 and Para [0032] Line 11 – 14: a signature along with associated data record is stored for validation purpose); and checking the identifier when calling up the at least one data record from the functional memory (Westendorf : Para [0036] Line 32 – 35: the data record request (i.e. calling up the data record) needs to be validated again using identifiers after a predetermined period of time).

8. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grawrock (U.S. Patent 6,678,833), in view of Westendorf et al. (U.S. Patent 2002/0042878), and in view of Jablon et al. (U.S. Patent 5,421,006).

As per claim 17 and 18, Grawrock as modified teaches storing a code word in a code word memory of the processor unit (Westendorf : Para [0026] Line 11 – 17: checksum is used for validation); and comparing the identifier with at least one of the code words; and determining a presence of validity when the at least one of the code words and the identifier match (Westendorf: Para [0035]).

However, Grawrock as modified does not disclose expressly storing a list of code words in a code word memory of the processor unit.

Jablon teaches storing a list of code words in a code word memory of the processor unit (Jablon : Column 17 Line 48 – 51, Column 8 Line 49 – 50 and Column 5 Line 32 – 35 & Figure 6 / Element 148: a list of MDC (Modification Detection Codes), e.g. checksums, is stored in NVM memory, which is considered as the code word memory).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teaching of Jablon within the system of Grawrock as modified because (a) Grawrock teaches a processor boot block identifier is calculated and used for data validation purpose (Grawrock : Column 3 Line 64 – 65) and (b) Jablon teaches an improved mechanism for assessing the software integrity during the system initialization and for verifying the boot record (Jablon : Column 1 Line 10 – 16 and Column 11 Line 59 – 67).

9. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Grawrock (U.S. Patent 6,678,833), in view of Westendorf et al. (U.S. Patent 2002/0042878), in view of Jablon et al. (U.S. Patent 5,421,006), and in view of Trang (U.S. Patent 5,630,054).

As per claim 19, Grawrock as modified does not teach storing a counter content of a counter, wherein the counter points to one of the code words of the code word memory; and incrementing the counter content of the counter before each check of the identifier of the at least one data record stored in the buffer memory.

Trang teaches storing a counter content of a counter, wherein the counter points to one of the code words of the code word memory (Trang : Column 6 Line 39 – 43); and incrementing the counter content of the counter before each check of the identifier of the at least one data record stored in the buffer memory (Trang : Column 6 Line 36 – 43).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teaching of Trang within the system of Grawrock as modified because (a) Grawrock teaches a processor boot block identifier is calculated and used for data validation purpose (Grawrock : Column 3 Line 64 – 65) and (b) Trang teaches an effective mechanism for storing and retrieving data error check information used to verify whether data record stored in the system contains errors (Trang : Column 1 Line 10 – 13).

10. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Grawrock (U.S. Patent 6,678,833), in view of Westendorf et al. (U.S. Patent 2002/0042878), and in view of Trang (U.S. Patent 5,630,054).

As per claim 22, Grawrock as modified teaches retrievably storing identifiers in a code word server (Westendorf : Para [0008] Line 5 – 6 and Para [0030] Line 19 – 24: a database of a central service of office stores identifiers for the processor unit) and the identifiers being allocatable to the processor unit via an identification sequence (Westendorf : Para [0026] Line 11 – 17: processor ID is also used for validation purpose).

However, Grawrock as modified does not disclose expressly a plurality of counter contents of a counter associated with identifiers.

Trang teaches a plurality of counter contents of a counter associated with identifiers (Trang : Column 6 Line 39 – 43).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teaching of Trang within the system of Grawrock as modified because (a) Grawrock teaches a processor boot block identifier is calculated and used for data validation purpose (Grawrock : Column 3 Line 64 – 65) and (b) Trang teaches an effective mechanism for storing and retrieving data error check information used to verify whether data record stored in the system contains errors (Trang : Column 1 Line 10 – 13).

11. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Westendorf et al. (U.S. Patent 2002/0042878), in view of Trang (U.S. Patent 5,630,054), and in view of Osthoff et al. (U.S. Patent 2002/0147918).

As per claim 24, Westendorf teaches wherein the processor unit is individualized via an identification sequence (Westendorf : Para [0026] Line 11 – 17: processor ID is also used for validation purpose).

However, Westendorf does not disclose expressly a read-only code word memory for storing code words; and a counter including an incrementable counter content that points to one of the code words, wherein the processor unit is individualized via an identification sequence.

Trang teaches a counter including an incrementable counter content that points to one of the code words (Trang : Column 6 Line 36 – 43).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teaching of Trang within the system of Westendorf because (a) Westendorf teaches an data validation method on data transfer by using an identifier such as cross-checksum (Westendorf : Para [0026] Line 10 – 17) and (b) Trang teaches an effective mechanism for storing and retrieving data error check information (i.e. checksum data) used to verify whether data record stored in the system contains errors (Trang : Column 1 Line 10 – 13).

Westendorf as modified does not disclose expressly a read-only code word memory for storing code words.

Osthoff teaches a read-only code word memory for storing code words (Osthoff: Para [0003]: securing a hash value in read-only memory).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teaching of Osthoff within the system of Westendorf as modified because (a) Westendorf teaches an data validation method on data transfer by using an identifier such as cross-checksum (Westendorf : Para [0026] Line 10 – 17) and (b) Osthoff teaches an improved mechanism for securing information in memory and, more specifically, for ensuring the security of stored information by securing a hash value in read-only memory (Osthoff: Para [0003]).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Longbit Chai whose telephone number is 571-272-3788. The examiner can normally be reached on Monday-Friday 8:00am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz R. Sheikh can be reached on 571-272-3795. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Longbit Chai, Ph.D.
Patent Examiner
Art Unit 2131
6/20/2007